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| EXAMINER |
|---|
| BROCK II, PAUL E |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/351,544 | CARNS ET AL. | |
| | Examiner | Art Unit | |
| | Paul E Brock II | 2815 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 July 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *3-11,15-30 and 36-71* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-11,15-30 and 36-71* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *26 February 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## DETAILED ACTION

1. The declaration under 37 CFR 1.132 filed July 30, 2002 is sufficient to overcome the rejection of claims 3 – 11, 15 – 30 and 36 – 42 based upon the previous U.S.C. sections 102 and 103 rejections in the office action filed May 3, 2002 based on Kayanuma and Takahashi because the silicide layers of the references are not the same as the anti-reflective layer claimed.

### *Drawings*

2. The corrected or substitute drawings were received on February 26, 2002. These drawings are approved.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 3 – 11, 15 – 25, 36 – 39 and 43 – 64 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claims 3 and 4 recites the limitation "the resultant structure" in lines 15 of the claims. There is insufficient antecedent basis for this limitation in the claim.

6. Claim 15 recites the limitation "the resultant structure" in line 14 of the claim. There is insufficient antecedent basis for this limitation in the claim.

7. Claim 36 recites the limitation "the structure resultant from" in lines 9 and 10. There is insufficient antecedent basis for this limitation in the claim. Further, it is not clear if the two recitations of "the structure resultant from" are referring to the same structure.

8. Claim 43 recites the limitation "the resultant structure" in line 16 and again in lines 17 and 18 of the claim. There is insufficient antecedent basis for this limitation in the claim. Further, it is not clear if the two recitations of "the resultant structure" are referring to the same structure.

9. Claim 48 recites the limitation "the resultant structure" in line 14. There is insufficient antecedent basis for this limitation in the claim.

10. Claim 49 recites the limitation "the resultant structure" in line 3. There is insufficient antecedent basis for this limitation in the claim. Further, it is not clear if the recitation of "the resultant structure" is referring to the same "resultant structure" as recited in claim 48, from which claim 49 depends.

11. Claim 52 recites the limitation "the resultant structure" in line 14 and again in line 16 of the claim. There is insufficient antecedent basis for this limitation in the claim. Further, it is not clear if the two recitations of "the resultant structure" are referring to the same structure.

12. Claim 59 recites the limitation "the resultant structure" in line 14. There is insufficient antecedent basis for this limitation in the claim.

13. Claim 60 recites the limitation "the resultant structure" in line 3. There is insufficient antecedent basis for this limitation in the claim. Further, it is not clear if the recitation of "the resultant structure" is referring to the same "resultant structure" as recited in claim 59, from which claim 60 depends.

14. For purposes of this office action "the resultant structure" or "the structure resulted from" will be considered the structure which was described preceding the recitation of the "resultant" phrase.

***Claim Rejections - 35 USC § 103***

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 3, 8 – 11, 36, 39, 40, 48, 49 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi (USPAT 5683931) in view of Bencher et al. ("Dielectric Antireflective coatings for DUV Lithography", Solid State Technology, March 1997, p. 109, Bencher).

With regard to claim 3, Takahashi discloses in figures 2a – 2e forming a capacitor in an integrated circuit. Takahashi discloses in figure 2a forming a bottom electrode layer (304) on a semiconductor body (301). Takahashi discloses in figure 2b forming a dielectric layer (305) over at least a portion of the bottom electrode. Takahashi discloses in figure 2b forming a top electrode layer (306) over at least a portion of the dielectric layer. Takahashi discloses in figure 2c removing a portion of the top electrode layer to expose a portion of the dielectric layer and subsequently removing at least a portion of the exposed portion of the dielectric layer to expose a portion of the lower electrode. Takahashi discloses in figure 2d subsequently forming a conformal insulating layer (307) over at least a portion of the exposed portion of the bottom electrode layer proximate to the exposed dielectric layer, the exposed dielectric layer and at least part of the top electrode layer proximate to the exposed dielectric layer. Takahashi discloses in figure 2e etching the bottom electrode layer using a photolithographic mask (309) subsequent to forming the conformal insulating layer. Takahashi is silent to teaching forming an anti-reflective layer (ARL) over at least a portion of the resultant structure subsequent to forming the conformal insulating layer. Bencher teaches in the last paragraph before the Dielectric ARC Design section forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of a resultant structure. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the antireflective layer of Bencher subsequent to forming

the conformal insulating layer and before forming the photolithographic mask in the method of Takahashi in order to easily maintain critical dimension (CD) control during pattern transfer in a photolithographic step as stated by Bencher in the last paragraph before the Dielectric ARC Design section.

With regard to claim 8, Bencher teaches in the last paragraph before the Dielectric ARC Design section wherein the ARL is an anti-reflective coating.

With regard to claim 9, Bencher teaches in the first paragraph after the Dielectric ARC Design section wherein the ARL is titanium nitride.

With regard to claim 10, Bencher teaches in the first sentence of the article wherein the ARL is a plasma enhanced chemical vapor deposition anti-reflective layer (PEARL).

With regard to claim 11, Bencher teaches in the last paragraph before the Dielectric ARC Design section wherein the plasma enhanced chemical vapor deposition anti-reflective layer has a thickness of 300 angstroms.

With regard to claim 36, Takahashi discloses in figure 2b forming a conductive layer on a semiconductor body. Takahashi discloses in figure 2c forming a capacitor structure comprising: a top electrode over a portion of the conductive layer; and a dielectric layer between the top electrode and the conductive layer. Takahashi discloses in figure 2d forming a conformal insulating layer over the capacitor structure and at least a portion of the conductive layer proximate to the capacitor structure. Takahashi discloses in figure 2e forming a patterned mask over the structure resultant from the forming a conformal insulating layer. Takahashi is silent to teaching forming an anti-reflective layer (ARL) over at least a portion of the resultant structure resultant from forming the conformal insulating layer before forming the patterned mask.

Bencher teaches in the last paragraph before the Dielectric ARC Design section forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of a resultant structure before forming a patterned mask. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the antireflective layer of Bencher on the structure resultant from the forming the conformal insulating layer and before forming the patterned mask in the method of Takahashi in order to easily maintain critical dimension (CD) control during pattern transfer in a photolithographic (patterning the mask) step as stated by Bencher in the last paragraph before the Dielectric ARC Design section. Takahashi discloses in figure 2e etching the conductive layer using the patterned mask.

With regard to claim 39, Takahashi discloses in figure 2e wherein the conductive layer is additionally used to form the gate of one or more transistors formed on the integrated circuit.

With regard to claim 40, Takahashi discloses in figure 2a forming a conductive layer on a semiconductor body. Takahashi discloses in figures 2a – 2f providing a process flow for etching the conductive layer, whereby the gates of one of more transistors are formed, the flow including a photolithographic process. Takahashi discloses in figures 2a – 2f a photolithographic process optimized for forming the gates. Takahashi is silent to forming an anti-reflective layer (ARL) over at least a portion of the conductive layer. Bencher teaches in the last paragraph before the Dielectric ARC Design section forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of a conductive layer. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the antireflective layer of Bencher over at least a portion of the conductive layer in the method of Takahashi in order to easily maintain critical dimension (CD) control during pattern transfer in a

photolithographic step as stated by Bencher in the last paragraph before the Dielectric ARC Design section. Takahashi discloses in figure 2e forming a patterned mask. It is further obvious in the method of Takahashi and Bencher that the patterned mask is formed over the ARL, wherein the photolithographic process is optimized for forming the gates. Takahashi discloses in figure 2a – 2e performing a capacitor formation process. Takahashi discloses in figures 2a – 2e forming one or more capacitor structures, each comprising a top electrode over a portion of the conductive layer and a dielectric layer between the top electrode and the conductive layer. Takahashi discloses in figures 2a – 2e forming a conformal insulating layer over the capacitor structures and at least a portion of the conductive layer proximate to capacitor structures and whereby the conformal insulating layer is formed such that the provided process flow is unaltered. It is further obvious in the method of Takahashi and Bencher that therein the capacitor formation process is performed prior to forming the ARL, whereby the ARL is additionally formed over the capacitor structures. Takahashi discloses in figure 2e etching the conductive layer according to the process flow, whereby the lower electrodes of the capacitor structures and the gates are formed.

Claim 48 is rejected similar to claim 3 as applied to Takahashi and Bencher with the additional limitation of: Bencher discloses in the Step 2 section under Dielectric ARC Design wherein the anti-reflective layer is a $Si_xON_y$ film.

With regard to claim 49, it is further obvious in the method of Takahashi and Bencher that the photoresist layer is formed over at least a portion of the resultant structure including the antireflective layer; and Bencher teaches in the third paragraph irradiating the photoresist.

With regard to claim 51, Bencher teaches in the last paragraph before the Dielectric ARC Design section wherein the anti-reflective layer has a thickness of 300 angstroms.

17. Claims 4 – 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi in view of Bencher and Wang et al. (USPAT 5545585, Wang).

With regard to claim 4, Takahashi discloses in figures 2a – 2e forming a capacitor in an integrated circuit. Takahashi discloses in figure 2a forming a bottom electrode layer (304) on a semiconductor body (301). Takahashi discloses in figure 2b forming a dielectric layer (305) over at least a portion of the bottom electrode. Takahashi discloses in figure 2b forming a top electrode layer (306) over at least a portion of the dielectric layer. Takahashi discloses in figure 2c removing a portion of the top electrode layer to expose a portion of the dielectric layer and subsequently removing at least a portion of the exposed portion of the dielectric layer to expose a portion of the lower electrode. Takahashi discloses in figure 2d subsequently forming a conformal insulating layer (307) over at least a portion of the exposed portion of the bottom electrode layer proximate to the exposed dielectric layer, the exposed dielectric layer and at least part of the top electrode layer proximate to the exposed dielectric layer. Takahashi discloses in figure 2e etching the bottom electrode layer using a photolithographic mask (309) subsequent to forming the conformal insulating layer. Takahashi is silent to teaching forming an anti-reflective layer (ARL) over at least a portion of the resultant structure subsequent to forming the conformal insulating layer. Bencher teaches in the last paragraph before the Dielectric ARC Design section forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of a resultant structure. It would have been obvious to one of ordinary skill in the art at

the time of the present invention to use the antireflective layer of Bencher subsequent to forming the conformal insulating layer and before forming the photolithographic mask in the method of Takahashi in order to easily maintain critical dimension (CD) control during pattern transfer in a photolithographic step as stated by Bencher in the last paragraph before the Dielectric ARC Design section. Takahashi and Bencher are silent to the conformal insulating layer having a thickness in the range of from 20 Å to 70 Å. Wang discloses in figure 7, column 7, lines 65 – 67 and column 8, lines 1 – 16 a conformal insulating layer (42) that has a thickness of 45 Å. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the thickness of the conformal insulating layer of Wang in the method of Takahashi and Bencher in order to form a material of high dielectric constant that is compatible with ULSI polysilicon processing as stated by Wang in column 1, lines 16 – 17, column 7, lines 65 – 67 and column 8, lines 1 – 16.

With regard to claim 5, Wang discloses in column 7, lines 65 – 67 and column 8, lines 1 – 16 wherein the conformal insulating layer is an oxide layer is formed in a thermal process.

With regard to claim 6, Wang discloses in column 7, lines 65 – 67 and column 8, lines 1 – 16 wherein the thermal process is a thermal oxidation. Takahashi, Bencher and Wang do not disclose that the conformal insulating layer is formed in a rapid thermal process that is a rapid thermal oxidation performed for a length of time in the range of from 10 to 60 seconds and at a temperature in the range from 850°C the 1050°C. It is well known in the art to use a rapid thermal process in the production of a thermal oxide layer that has parameters of from 10 to 60 seconds and at a temperature in the range from 850°C the 1050°C. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use a rapid thermal

process that has parameters of from 10 to 60 seconds and at a temperature in the range from 850°C the 1050°C to form the conformal insulating layer of Takahashi, Bencher and Wang in order to choose a method that is widely used and understood in the art and produces a consistent and reliable oxide layer.

With regard to claim 7, Wang discloses in column 7, lines 65 – 67 and column 8, lines 1 – 16 wherein the conformal insulating layer is formed by deposition.

18. Claims 15, 16, 19 – 25 and 59 – 64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kayanuma et al. (USPAT 5397729, Kayanuma) in view of Bencher.

In regard to claim 15, Kayanuma discloses in figures 4a – 4f and column 10, lines 38 – 40 forming a capacitor in an integrated circuit. Kayanuma discloses in figure 4a forming a bottom electrode layer (52) on a semiconductor body (50). Kayanuma discloses in figure 4a forming a dielectric layer (53) over at least a portion of the bottom electrode. Kayanuma discloses in figure 4a forming a top electrode layer (54) over at least a portion of the dielectric layer. Kayanuma discloses in figure 4b and column 10, lines 38 – 40 removing a portion of the top electrode layer to expose a portion of the dielectric layer. Kayanuma discloses in figure 4c and column 10, lines 38 – 40 forming an insulating layer (57) over at least a portion of the top electrode layer and the exposed portion of the dielectric layer. Kayanuma discloses in figure 4d removing a portion of the insulating layer and a portion of the dielectric layer, thereby exposing at least a portion of the lower electrode and forming side wall spacers , wherein the side wall spacers are formed on the side walls of the top electrode and of the inter electrode region of the dielectric. Kayanuma discloses in figures 4d – 4e etching the bottom electrode layer using a photolithographic mask

(60) subsequent to removing a portion of the insulating layer. Kayanuma is silent to teaching forming a non-insulating layer over at least a portion of the resultant structure subsequent to removing a portion of the insulating layer and a portion of the dielectric layer, wherein the non-insulating layer is an anti-reflective layer (ARL) for use in a photolithographic process. Bencher teaches in the last paragraph before the Dielectric ARC Design section forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of a resultant structure. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the non-insulating layer of Bencher that is an anti-reflective layer for use in a photolithographic step subsequent to removing a portion of the insulating layer and a portion of the dielectric layer and before forming the photolithographic mask in the method of Kayanuma in order to easily maintain critical dimension (CD) control during pattern transfer in a photolithographic step as stated by Bencher in the last paragraph before the Dielectric ARC Design section.

With regard to claim 16, Kayanuma discloses in column 8, lines 48 – 52 wherein the insulating layer is formed by deposition.

With regard to claim 19, Kayanuma discloses in column 8, lines 48 – 52 wherein the insulating layer is an oxide layer with a thickness of 1000 Å.

With regard to claim 20, Kayanuma discloses in column 8, lines 33 – 36 and 48 – 52 wherein the side wall spacers have a width in the range of about 1450 Å.

With regard to claim 21, Bencher teaches in the last paragraph before the Dielectric ARC Design section wherein the ARL is an anti-reflective coating.

With regard to claim 22, Bencher teaches in the first paragraph after the Dielectric ARC Design section wherein the ARL is titanium nitride.

With regard to claim 23, Bencher teaches in the first sentence of the article wherein the ARL is a plasma enhanced chemical vapor deposition anti-reflective layer (PEARL).

With regard to claim 24, Bencher teaches in the last paragraph before the Dielectric ARC Design section wherein the plasma enhanced chemical vapor deposition anti-reflective layer has a thickness of 300 angstroms.

With regard to claim 25, Kayanuma discloses in figure 4f wherein the bottom electrode layer is additionally used to form the gate of one or more transistors formed on the integrated circuit.

Claim 59 is rejected similar to claim 15 as applied to Kayanuma and Bencher with the additional limitation of: Bencher discloses in the Step 2 section under Dielectric ARC Design wherein the anti-reflective layer is a $Si_xON_y$ film.

With regard to claim 60, it is further obvious in the method of Kayanuma and Bencher that the photoresist layer is formed over at least a portion of the resultant structure including the antireflective layer; and Bencher teaches in the third paragraph irradiating the photoresist.

With regard to claim 61, Kayanuma discloses in column 8, lines 48 – 52 wherein the insulating layer is an oxide layer with a thickness of 1000 Å.

With regard to claim 62, Kayanuma discloses in column 8, lines 33 – 36 and 48 – 52 wherein the side wall spacers have a width in the range of about 1450 Å.

With regard to claim 63, Bencher teaches in the last paragraph before the Dielectric ARC Design section wherein the anti-reflective layer has a thickness of 300 angstroms.

With regard to claim 64, Kayanuma discloses in figure 4f wherein the bottom electrode layer is additionally used to form the gate of one or more transistors formed on the integrated circuit.

19. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kayanuma and Bencher as applied to claims 15 and 16 above, and further in view of Patel et al. (USPAT 5374578, Patel).

Kayanuma and Bencher do not teach wherein prior to forming the insulating layer by deposition, an anneal is performed. Patel teaches in figures 6 and 7 and column 5, lines 13 – 18 prior to forming an insulating layer (18) by deposition, an anneal is performed. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the anneal of Patel in the method of Kayanuma in order to reduce electrode and material deficiencies as stated by Kayanuma in column 1, lines 13 – 17.

20. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kayanuma and Bencher as applied to claim 15, above, and further in view of Wang.

With regard to claim 18, Kayanuma and Bencher do not disclose wherein the insulating layer is grown. Wang discloses in column 7, lines 65 – 67 and column 8, lines 1 – 16 growing an insulating layer. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use method of growing an insulating layer of Wang in the method of Kayanuma in order to form a material of high dielectric constant that is compatible with polysilicon processing as stated by Wang in column 7, lines 65 – 67 and column 8, lines 1 – 16.

21. Claims 26 – 30 and 69 – 71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. (USPAT 5618749, $Takahashi_2$) in view of Bencher.

With regard to claim 26, $Takahashi_2$ discloses in figures 6 – 10 a method of forming a capacitor in an integrated circuit. $Takahashi_2$ discloses in figure 6 forming a bottom electrode layer (2) on a semiconductor body (100). $Takahashi_2$ discloses in figure 7 forming a dielectric layer (1) over at least a portion of the bottom electrode. $Takahashi_2$ discloses in figure 7 forming a top electrode layer (6a) over at least a portion of the dielectric layer. $Takahashi_2$ discloses in figure 8 removing a portion of the top electrode layer to expose a portion of the dielectric layer. $Takahashi_2$ discloses in figure 10 subsequently forming a photolithographic mask (7a and 7b) and removing a portion of the exposed portion of the dielectric layer and a portion of the bottom electrode layer, thereby exposing at least a portion of the semiconductor body and forming one or more capacitors. $Takahashi_2$ is silent to forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of the top electrode and the exposed portion of the dielectric layer before the step of forming the photolithographic mask. Bencher teaches in the last paragraph before the Dielectric ARC Design section forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of a resultant structure. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the antireflective layer of Bencher before forming the photolithographic mask in the method of $Takahashi_2$ in order to easily maintain critical dimension (CD) control during pattern transfer in a photolithographic step as stated by Bencher in the last paragraph before the Dielectric ARC Design section.

With regard to claim 27, Bencher teaches in the last paragraph before the Dielectric ARC Design section wherein the ARL is an anti-reflective coating.

With regard to claim 28, Bencher teaches in the first paragraph after the Dielectric ARC Design section wherein the ARL is titanium nitride.

With regard to claim 29, Bencher teaches in the first sentence of the article wherein the ARL is a plasma enhanced chemical vapor deposition anti-reflective layer (PEARL).

With regard to claim 30, Takahashi$_2$ discloses in figure 10 wherein the bottom electrode layer is additionally used to form the gate of one or more transistors formed on the integrated circuit.

Claim 69 is rejected similar to claim 26 as applied to Takahashi$_2$ and Bencher with the additional limitation of: Bencher discloses in the Step 2 section under Dielectric ARC Design wherein the anti-reflective layer is a $Si_xON_y$ film.

With regard to claim 70, it is further obvious in the method of Takahashi$_2$ and Bencher that the photoresist layer is formed over at least a portion of the antireflective layer; and Bencher teaches in the third paragraph irradiating the photoresist. Takahashi$_2$ discloses in figure 10 wherein the removing a portion of the exposed portion of the dielectric layer and a portion of the bottom electrode layer is performed using the photoresist.

With regard to claim 71, Takahashi$_2$ discloses in figure 10 wherein the bottom electrode layer is additionally used to form the gate of one or more transistors formed on the integrated circuit.

22. Claims 37, 38, 41, 42 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahasi and Bencher as applied to claims 36, 40 and 48 above, and further in view of Wang.

With regard to claims 37, 41 and 50, Takahasi and Bencher do not disclose that the conformal insulating layer has a thickness in the range of from 20 Å to 70 Å. Wang discloses in figure 7, column 7, lines 65 – 67 and column 8, lines 1 – 16 a conformal insulating layer (42) that has a thickness of 45 Å. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the thickness of the conformal insulating layer of Wang in the method of Takahasi and Bencher in order to form a material of high dielectric constant that is compatible with polysilicon processing as stated by Wang in column 7, lines 65 – 67 and column 8, lines 1 – 16.

With regard to claims 38 and 42, Wang discloses in column 7, lines 65 – 67 and column 8, lines 1 – 16 wherein the conformal insulating layer is an oxide layer is formed in a thermal process.

23. Claims 43, 44, 46 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi in view of Bencher and the applicant's admitted prior art (AAPA).

Claim 43 is rejected similar to claim 3 as applied to Takahashi and Bencher with the additional limitations of: It is further obvious in the method of Takahashi and Bencher wherein the photoresist is subsequently formed over at least a portion of the resultant structure including the anti-reflective layer; and Bencher teaches in the third paragraph irradiating the photoresist. It is not clear if Takahashi and Bencher teach wherein the antireflective layer reduces the

reflectivity to the radiation that penetrates the photoresist by 70% or more. The AAPA teaches on page 1, lines 23 – 24 and page 2, lines 1 – 6 wherein an antireflective layer reduces the reflectivity to a radiation that penetrates a photoresist by 70% or more. It would have been obvious to use the antireflective layer of the AAPA in the method of Takahashi and Bencher in order to substantially reduce standing waves as stated by the AAPA on page 1, lines 23 – 24 and page 2, lines 1 – 6.

With regard to claim 44, the AAPA teaches on page 1, lines 23 – 24 and page 2, lines 1 – 6 wherein the anti-reflective layer reduces the reflectivity to the radiation that penetrates the photoresist by 71%.

With regard to claim 46, Bencher discloses in the Step 2 section under Dielectric ARC Design wherein the anti-reflective layer is a $Si_xON_y$ film.

With regard to claim 47, Bencher teaches in the last paragraph before the Dielectric ARC Design section wherein the anti-reflective layer has a thickness of 300 angstroms.

24. Claim 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahasi, Bencher and the AAPA as applied to claim 43 above, and further in view of Wang.

With regard to claim 45, Takahasi and Bencher do not disclose that the conformal insulating layer has a thickness in the range of from 20 Å to 70 Å. Wang discloses in figure 7, column 7, lines 65 – 67 and column 8, lines 1 – 16 a conformal insulating layer (42) that has a thickness of 45 Å. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the thickness of the conformal insulating layer of Wang in the method of Takahasi and Bencher in order to form a material of high dielectric constant that is compatible

with polysilicon processing as stated by Wang in column 7, lines 65 – 67 and column 8, lines 1 – 16.

25. Claims 52 – 58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kayanuma in view of Bencher and the AAPA.

Claim 52 is rejected similar to claim 15 as applied to Kayanuma and Bencher with the additional limitations of: It is further obvious in the method of Kayanuma and Bencher wherein the photoresist is subsequently formed over at least a portion of the resultant structure including the anti-reflective layer; and Bencher teaches in the third paragraph irradiating the photoresist. It is not clear if Kayanuma and Bencher teach wherein the antireflective layer reduces the reflectivity to the radiation that penetrates the photoresist by 70% or more. The AAPA teaches on page 1, lines 23 – 24 and page 2, lines 1 – 6 wherein an antireflective layer reduces the reflectivity to a radiation that penetrates a photoresist by 70% or more. It would have been obvious to use the antireflective layer of the AAPA in the method of Kayanuma and Bencher in order to substantially reduce standing waves as stated by the AAPA on page 1, lines 23 – 24 and page 2, lines 1 – 6.

With regard to claim 53, the AAPA teaches on page 1, lines 23 – 24 and page 2, lines 1 – 6 wherein the anti-reflective layer reduces the reflectivity to the radiation that penetrates the photoresist by 71%.

With regard to claim 54, Kayanuma discloses in column 8, lines 48 – 52 wherein the insulating layer is an oxide layer with a thickness of 1000 Å.

With regard to claim 55, Kayanuma discloses in column 8, lines 33 – 36 and 48 – 52 wherein the side wall spacers have a width in the range of about 1450 Å.

With regard to claim 56, Bencher discloses in the Step 2 section under Dielectric ARC Design wherein the anti-reflective layer is a $Si_xON_y$ film.

With regard to claim 57, Bencher teaches in the last paragraph before the Dielectric ARC Design section wherein the anti-reflective layer has a thickness of 300 angstroms.

With regard to claim 58, Kayanuma discloses in figure 4f wherein the bottom electrode layer is additionally used to form the gate of one or more transistors formed on the integrated circuit.

26. Claims 65 – 68 are rejected under 35 U.S.C. 103(a) as being unpatentable over $Takahashi_2$ in view of Bencher and the applicant's admitted prior art (AAPA).

Claim 65 is rejected similar to claim 26 as applied to $Takahashi_2$ and Bencher with the additional limitations of: It is further obvious in the method of $Takahashi_2$ and Bencher wherein the photoresist is subsequently formed over at least a portion of the resultant structure including the anti-reflective layer; and Bencher teaches in the third paragraph irradiating the photoresist. It is not clear if $Takahashi_2$ and Bencher teach wherein the antireflective layer reduces the reflectivity to the radiation that penetrates the photoresist by 70% or more. The AAPA teaches on page 1, lines 23 – 24 and page 2, lines 1 – 6 wherein an antireflective layer reduces the reflectivity to a radiation that penetrates a photoresist by 70% or more. It would have been obvious to use the antireflective layer of the AAPA in the method of Takahashi and Bencher in

order to substantially reduce standing waves as stated by the AAPA on page 1, lines 23 – 24 and page 2, lines 1 – 6.

With regard to claim 66, the AAPA teaches on page 1, lines 23 – 24 and page 2, lines 1 – 6 wherein the anti-reflective layer reduces the reflectivity to the radiation that penetrates the photoresist by 71%.

With regard to claim 67, Bencher discloses in the Step 2 section under Dielectric ARC Design wherein the anti-reflective layer is a $Si_xON_y$ film.

With regard to claim 68, Takahashi$_2$ discloses in figure 10 wherein the bottom electrode layer is additionally used to form the gate of one or more transistors formed on the integrated circuit.

***Response to Arguments***

27. Applicant's arguments filed July 30, 2002 have been fully considered but they are not persuasive.

28. In response to applicant's argument that an anti-reflective layer is used as part of a photolithographic process, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
September 6, 2002

GEORGE C. ECKERT II
PATENT EXAMINER